LVDS Output Modes on the HMCAD15xx and HMCAD11xx ADCs

Product Application Note

© 2012 Hittite Microwave Corporation, All Rights Reserved.
2 Elizabeth Drive Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373

Contents

Tables

© 2012 Hittite Microwave Corporation, All Rights Reserved.
2 Elizabeth Drive Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373

1 Introduction

The LVDS output control and configuration for the HMCAD15xx and HMCAD11xx series of Analog to Digital Converters is a topic covered in detail in the respective data sheets for those parts.

The following tables present a summary of the available LVDS output modes, maximum sample rate, and bit and clock rates. These are dependent on the number of channels used, the data precision (1520) and the choice of DDR or SD operation (11xx).

2 HMCAD1520 DDR LVDS Output Modes

For the HMCAD1520, 12-bit LVDS mode is default for all operational modes. If another LVDS mode is to be used, the *lvds_output_mode* register setting must be changed accordingly. When 8-bit LVDS mode is used, the LSBs are truncated and the data output will have 8-bit resolution. When 14 or 16 bit LVDS output mode is selected the output data will be a 13 bit left justified word filled up with '0's on the LSB side.

2.1 HMCAD1520 High Speed Mode

LVDS Output	**High Speed Mode (12 bit Res)**	1 channel	2 channels	4 channels
8 bit	Maximum Sample Rate	1000 MSPS	500 MSPS	250 MSPS
	LVDS Pairs (per channel)	8	4	2
	Total Bit Rate (per channel)	8 GBPS	4 GBPS	2 GBPS
	Bit Rate (per pair)	1 GBPS	1 GBPS	1 GBPS
	Lclk	500 MHz	500 MHz	500 MHz
	Fclk	125 MHz	125 MHz	125 MHz
	Prop Delay (samples)	128	64	32
12 bit	Maximum Sample Rate	640 MSPS	320 MSPS	160 MSPS
	LVDS Pairs (per channel)	8	4	2
	Total Bit Rate (per channel)	7.68 GBPS	3.84 GBPS	1.92 GBPS
	Bit Rate (per pair)	960 MBPS	960 MBPS	960 MBPS
	Lclk	480 MHz	480 MHz	480 MHz
	Fclk	80 MHz	80 MHz	80MHz
	Prop Delay (samples)	128	64	32

Table 1 HMCAD1520 LVDS High Speed Modes

© 2012 Hittite Microwave Corporation, All Rights Reserved.
2 Elizabeth Drive Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373

2.2 HMCAD1520 Precision Mode

LVDS Output	**Precision Mode (14 bit Res)**	4 channels	
14 bit	Maximum Sample Rate	70 MSPS	
	LVDS Pairs (per channel)	1	
	Total Bit Rate (per channel)	.98 GBPS	
	Bit Rate (per pair)	.98 GBPS	
	Lclk	490 MHz	
	Fclk	70 MHz	
	Prop Delay (samples)	15	
16 bit	Maximum Sample Rate	62.5 MSPS	
	LVDS Pairs (per channel)	1	
	Total Bit Rate (per channel)	1.00 GSPS	
	Bit Rate (per pair)	1.00 GSPS	
	Lclk	500 MHz	
	Fclk	62.5 MHz	
	Prop Delay (samples)	15	
Dual 8 bit	Maximum Sample Rate	105 MSPS	125 MSPS*
	LVDS Pairs (per channel)	2	2
	Total Bit Rate (per channel)	1.68 GSPS	2.00 GBPS
	Bit Rate (per pair)	0.84 GSPS	1.00 GBPS
	Lclk	420 MHz	500 MHz
	Fclk	105 MHz	125 MHz
	Prop Delay (samples)	15	15

** Contact Hittite for Details*

Table 2 HMCAD1520 LVDS Precision Modes

© 2012 Hittite Microwave Corporation, All Rights Reserved.
2 Elizabeth Drive Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373

3 HMCAD1511, 1510 DDR LVDS Output Modes

The HMCAD1511 and HMCAD1510 only use an 8-bit LVDS output. The maximum sample rate is set by the number of channels used.

LVDS Output	**HMCAD1511 (8 bit Res)**	1 channel	2 channels	4 channels
8 bit	Maximum Sample Rate	1000 MSPS	500 MSPS	250 MSPS
	LVDS Pairs (per channel)	8	4	2
	Total Bit Rate (per channel)	8 GBPS	4 GBPS	2 GBPS
	Bit Rate (per pair)	1 GBPS	1 GBPS	1 GBPS
	Lclk	500 MHz	500 MHz	500 MHz
	Fclk	125 MHz	125 MHz	125 MHz
	Prop Delay (samples)	128	64	32
LVDS Output	**HMCAD1510 (8 bit Res)**	1 channel	2 channels	4 channels
8 bit	Maximum Sample Rate	500 MSPS	250 MSPS	125 MSPS
	LVDS Pairs (per channel)	8	4	2
	Total Bit Rate (per channel)	4 GBPS	2 GBPS	1 GBPS
	Bit Rate (per pair)	500 MBPS	500 MBPS	500 MBPS
	Lclk	250 MHz	250 MHz	250 MHz
	Fclk	62.5 MHz	62.5 MHz	62.5 MHz
	Prop Delay (samples)	128	64	32

Table 3 HMCAD1511, 1510 DDR LVDS Output Modes

4 HMCAD11xx DDR and SDR LVDS Output Modes

For the HMCAD11xx series, there are two options for the serial LVDS outputs, 12 bits or 14 bits. This is selected by setting *lvds_num_bits* to '0' or '1', respectively. In 12 bit mode, the LSB bit from the ADCs are removed in the output stream. In 14 bit mode, a '0' is added in the LSB position. The output interface of HMCAD11xx is normally a DDR interface; however, the device can also be made to operate in SDR mode by setting the *en_sdr* bit to '1'. The bit clock (LCLK) is output at 12x times the input clock in this mode, twice as fast as in DDR mode. The SDR mode is not recommended beyond 40 MSPS.

© 2012 Hittite Microwave Corporation, All Rights Reserved.
2 Elizabeth Drive Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373

LVDS Output	**HMCAD1102**	12 bit DDR	14 bit DDR	12 bit SDR
	Maximum Sample Rate	80 MSPS	65 MSPS	40 MSPS
	LVDS Pairs (per channel)	1	1	1
	Total Bit Rate (per channel)	960 MSPS	910 MSPS	480 MSPS
	Bit Rate (per pair)	960 MSPS	910 MSPS	480 MSPS
	Lclk	480 MHz	455 MHz	480 MHz
	Fclk	80 MHz	65 MHz	40 MHz
	Prop Delay (samples)	14	14	14
	Output Data Resolution	12	13	12
LVDS Output	**HMCAD1101**	12 bit DDR	14 bit DDR	12 bit SDR
	Maximum Sample Rate	65 MSPS	65 MSPS	40 MSPS
	LVDS Pairs (per channel)	1	1	1
	Total Bit Rate (per channel)	780 MSPS	910 MSPS	480 MSPS
	Bit Rate (per pair)	780 MSPS	910 MSPS	480 MSPS
	Lclk	390 MHz	455 MHz	480 MHz
	Fclk	65 MHz	65 MHz	40 MHz
	Prop Delay (samples)	14	14	14
	Output Data Resolution	12	13	12
LVDS Output	**HMCAD1100**	12 bit DDR	14 bit DDR	12 bit SDR
	Maximum Sample Rate	50 MSPS	50 MSPS	40 MSPS
	LVDS Pairs (per channel)	1	1	1
	Total Bit Rate (per channel)	600 MSPS	700 MSPS	480 MSPS
	Bit Rate (per pair)	600 MSPS	700 MSPS	480 MSPS
	Lclk	300 MHz	350 MHz	480 MHz
	Fclk	50 MHz	50 MHz	40 MHz
	Prop Delay (samples)	14	14	14
	Output Data Resolution	12	13	12

Table 4 HMCAD11xx DDR and SDR LVDS Output Modes

© 2012 Hittite Microwave Corporation, All Rights Reserved.
2 Elizabeth Drive Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373